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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,780	09/27/2005	Tetsuya Taki	PTGF-04041US	9224

21254 7590 11/28/2008

MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
GOODWIN, DAVID J	
ART UNIT	PAPER NUMBER
2818	
MAIL DATE	DELIVERY MODE
11/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,780	TAKI, TETSUYA	
	Examiner	Art Unit	
	DAVID GOODWIN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 through 3, 6 and 17are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 6,064,079) in view of Yamamoto (US 6,064,079) in view of Ikeda (US 2003/0059972).

3. Yamamoto teaches a group III nitride based semiconductor device (column 1 lines 45-60). Said device comprises a first p-layer (16) and a second p layer (18) comprising an acceptor impurity (column 4 lines 30-60). An intermediate layer (32) provided between the first p layer (16) and the second p layer (18) the intermediate layer (32) contacting a surface of the first p layer (16) and a surface of the second p layer (18). The intermediate layer (32) contacts an entirety of the surface of the second p layer (18) and an entirety of the surface of the first p layer (16) (fig 1a) (column 4 lines 35-65). The first p layer (16) is formed on the light emitting layer (14) the intermediate layer (32) is formed above the first p layer (16) and the second p layer (18) is formed above the intermediate layer (32).

4. Yammamoto does not teach that the intermediate layer comprises a donor impurity.

5. Yammamoto teaches a second embodiment comprising an intermediate layer (34) between a first p layer (15) and a second p layer (18). Said intermediate layer comprises a donor impurity (column 5 lines 25-55).

6. It would have been obvious to one of ordinary skill in the art to include donor dopant impurity into the intermediate layer in order to compensate for the p dopant and modulate the device.

7. Yamamoto does not teach the relative bandgaps of the first p layer, the intermediate layer and the second p layer.

8. Ikeda teaches forming a light emitting device comprising a first p layer, an intermediate layer and a second p layer formed over a light emitting layer. Wherein the band gap decreases from a position proximate the light emitting layer to a position proximate the second p layer (fig 11-13) (paragraph 32).

9. It would have been obvious to one of ordinary skill in the art to decrease the band gap in order to reduce the series resistance of the device.

10. Regarding claim 2.

11. Yamamoto teaches the donor impurity doped into the intermediate layer is doped with a concentration distribution corresponding to a concentration distribution of the acceptor impurity in the intermediate layer (fig 2B) (column 5 lines 35-60).

12. Regarding claim 3.

13. Yamamoto teaches the acceptor impurity is magnesium and the donor impurity is silicon (column 5 lines 10-45).

14. Regarding claim 6.

15. Yamamoto teaches the first p layer (15) includes a p cladding layer (15) made of p type AlGaN doped with Mg (column 5 lines 10-25). The second p-layer (18) includes a p contact layer (18) made of p type GaN doped with Mg (column 5 lines 10-30).

16. Regarding claim 17.

17. Yamamoto teaches that that said low an intermediate layer (32) with a low cionductivity which will allow current flow in an entire region thereof (fig 1a) (column 4 lines 35-65).

18. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 6,064,079) in view of Yamamoto (US 6,064,079) in view of Ikeda (US 2003/0059972) as applied to claim 1 above and further in view of Fukuda (JP2003-115610).

19. Regarding claim 4.

20. Yamamoto in view of Yamamoto in view of Ikeda teaches elements of the claimed invention above in the rejection of claim 1.

21. Yamamoto in view of Ikeda does not teach the relative concentrations of the dopants.

22. Fukuda teaches a group III nitride semiconductor device. Said device comprises intermediate layers having concentration of Mg dopant of 1E18/cm^3 and intermediate layers having silicon dopant concentration of 1E17/cm^3 (translation paragraphs 0010-0015). The ration of which is 10 to 1.

23. It would have been obvious to one of ordinary skill in the art to dope the intermediate layer with these concentrations in order to reduce current leakage without affecting the crystal structure.

24. Regarding claim 5.

25. The above concentrations of dopants will result in a hole density of less than 10^17/cm^3.

26. Claims 7 through 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 6,064,079) in view of Yamamoto (US 6,064,079) in view of Ikeda (US 2003/0059972) in view of Kaneyama (US 2002/0014632.

27. Regarding claim 7.

28. Yamamoto teaches that a group III nitride semiconductor device is formed on a sapphire substrate (10) (column 4 lines 25-45). An n contact layer (12) formed on the sapphire substrate (10) (column 4 lines 30-40). An n cladding layer (13) formed on the n contact layer (12) (column 4 lines 30-45). A light emitting layer (14) formed on the n cladding layer (13) (column 4 lines 30-50). A p cladding layer (15, 16) and a p type contact layer (18) to each of which an acceptor impurity is added (column 4 lines 35-55). An intermediate layer (32) provided between the p cladding layer (15, 16) and the p contact layer (18). A p electrode (22) is disposed on the p contact layer (18). An n electrode (21) disposed on the n contact layer (12).

29. Yammamoto does not teach that the intermediate layer comprises a donor impurity.

30. Yammaoto teaches a second embodiment comprising an intermediate layer (34) between a first p layer (15) and a second p layer (18). Said intermediate layer comprises a donor impurity (column 5 lines 25-55).

31. It would have been obvious to one of ordinary skill in the art to include donor dopant impurity into the intermediate layer in order to compensate for the p dopant and modulate the device.

32. Yamamoto does not teach the relative bandgaps of the first p layer, the intermediate layer and the second p layer.

33. Ikeda teaches forming a light emitting device comprising a first p layer, an intermediate layer and a second p layer formed over a light emitting layer. Wherein the band gap decreases from a position proximate the light emitting layer to a position proximate the second p layer (fig 11-13) (paragraph 32).

34. It would have been obvious to one of ordinary skill in the art to decrease the band gap in order to reduce the series resistance of the device.

35. Yamamoto does not teach that the p electrode comprises a thin film electrode and a thick film electrode.

36. Kaneyama teaches group III nitride semiconductor device comprises a contact layer (109). A thin film electrode (110) is disposed on said contact layer (109). A thick film electrode (120) is disposed on the thin film electrode (109) (fig 1) (paragraph 0036-0039).

37. It would have been obvious to one of ordinary skill in the art to form an electrode of a thin film and a thick film in order to form a good electrical connection without blocking the emitted light.

38. Regarding claim 8.

39. Yamamoto teaches that the light emitting includes a multi-quantum well structure (14) formed on the n cladding layer (13) by laminating multiple pairs of well layers of undoped InGaN and barrier layer of undoped GaN (column 4 lines 25-45).

40. Regarding claim 9.

41. Kaneyama teaches group III nitride semiconductor device comprises a contact layer (109). A thin film electrode (110) is disposed on said contact layer (109). Said thin film electrode (110) is formed of a layer of cobalt (111) and a second layer of gold (112) (paragraph 0038). A thick film p electrode (120) is disposed on the thin film electrode (109) (fig 1) (paragraph 0036-0039). Said thick film p electrode is formed by laminating a first layer of vanadium (121), a second layer of gold (122), and a third layer aluminum (123) sequence on the thin film p electrode (110) (paragraph 0039).

42. It would have been obvious to one of ordinary skill in the art to form an electrode of a thin film and a thick film in order to form a good electrical connection without blocking the emitted light.

43. Regarding claim 10.

44. Kaneyama teaches a reflective metal layer (150) of aluminum formed on the sapphire substrate (101) (paragraph 0040).

45. It would have been obvious to one of ordinary skill in the art to form a reflective metal layer in order to direct all emitted light in one direction thereby increasing the efficiency of the device.

46. Regarding claim 18.

47. Yamamoto teaches that that said low an intermediate layer (32) with a low cionductivity which will allow current flow in an entire region thereof (fig 1a) (column 4 lines 35-65).

48.

49. Claims 11 through 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 6,064,079) in view of Yamamoto (US 6,064,079) in view of Ikeda (US 2003/0059972) as applied to claim 1 above and further in view of Fukuda (JP2003-115610).

50. Regarding claim 11.

51. Yamamoto in view of Yamamoto in view of Ikeda teaches elements of the claimed invention above in the rejection of claim 1.

52. Yamamoto further teaches that the intermediate layer (32) has a high resistivity.

53. Yamamoto does not teach the relative concentrations of the dopants.

54. Fukuda teaches a group III nitride semiconductor device. Said device comprises intermediate layers having concentration of Mg dopant of 1E18/cm^3 and intermediate layers having silicon dopant concentration of 1E17/cm^3 (translation paragraphs 0010-0015). The ration of which is 10 to 1.

55. Further, an amount of donor impurity will inherently offset an amount of acceptor impurity.

56. It would have been obvious to one of ordinary skill in the art to dope the intermediate layer with these concentrations in order to reduce current leakage without affecting the crystal structure.

57. Regarding claim 12.

58. Fukuda teaches that the intermediate layer (11) is about 100 nm (table 1).

59. It would have been obvious to one of ordinary skill in the art to form an intermediate layer of about 100 nm in order to sufficient charge blocking to prevent current flow.

60. Regarding claim 13.

61. Yamamoto does not teach the relative concentrations of the dopants.

62. Fukuda teaches a group III nitride semiconductor device. Said device comprises intermediate layers having concentration of Mg dopant of 1E18/cm^3 and intermediate layers having silicon dopant concentration of 1E17/cm^3 (translation paragraphs 0010-0015). The ration of which is 10 to 1.

63. It would have been obvious to one of ordinary skill in the art to dope the intermediate layer with these concentrations in order to reduce current leakage without affecting the crystal structure.

64. Regarding claim 14.

65. Fukuda teaches a group III nitride semiconductor device. Said device comprises intermediate layers having concentration of Mg dopant of 1E18/cm^3 and intermediate

layers having silicon dopant concentration of 1E17/cm^3 (translation paragraphs 0010-0015). This results in the donor and acceptor activation rates being substantially equal.

66. It would have been obvious to one of ordinary skill in the art to dope the intermediate layer with these concentrations in order to reduce current leakage without affecting the crystal structure.

67. Claims 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 6,064,079) in view of Yamamoto (US 6,064,079) in view of Ikeda (US 2003/0059972) as applied to claim 1 above and further in view of Nomura (US 2003/0147440).

68. Regarding claim 15.

69. Yamaotoin view of Ikeda teaches elements of the claimed invention above.

70. Yamaoto in view of Ikeda does not teach the composition of the AlGaN cladding layer.

71. Nomura teaches an AlGaN cladding layer comprised of Al.sub.0.15Ga.sub.0.85N (paragraph 0062).

72. It would have been obvious to one of ordinary skill in the art to use a cladding layer of Al.sub.0.15Ga.sub.0.85N in order to have the proper bandgap for generating light.

73. Regarding claim 19.

74. Yamamoto teaches that that said low an intermediate layer (32) with a low cionductivity which will allow current flow in an entire region thereof (fig 1a) (column 4 lines 35-65).

75.

76. Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US 6,064,079) in view of Yamamoto (US 6,064,079) in view of Ikeda (US 2003/0059972) as applied to claim 1 above and further in view of Ishikawa (US 4,987,096).

77. Regarding claim 16.

78. Yamamoto in view of Yamamoto in view of Ikeda teaches elements of the claimed invention above.

79. Yamamoto in view of Yamamoto in view of Ikeda does not teach the concentration of dopant in the current blocking layer.

80. Ishikawa teaches a current blocking layer having a silicon dopant concentration of 2*10^18 cm-3.

81. It would have been obvious to one of ordinary skill in the art to dope to a concentration of 2*10^18 cm-3 in order to provide enough donors to block the acceptor charge carriers.

Response to Arguments

82. Applicant's arguments with respect to claims 1 through 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

83. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID GOODWIN whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

djg

/Steven Loke/

Supervisory Patent Examiner, Art Unit 2818